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## 15<sup>th</sup> ACM International Conference on Supercomputing



**Final Program**  
June 16-21, 2001  
Sorrento, Italy

**Sponsored by ACM/SIGARCH**

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Saturday, June 16		Sunday, June 17		
<p style="text-align: center;"><u>Tutorial</u></p> <p>IA-64 Architecture and Compiler Technology M. Serrano - Intel</p>		<p style="text-align: center;"><u>Workshops</u></p> <p>Java for High-Performance Computing Caching, Coherence and Consistency</p>		
Monday, June 18		Tuesday, June 19		
9:00	Conference Opening	<p><u>Session 4.1: Program Development Tools</u></p> <p>“Tools for Application-Oriented Performance Tuning” J. Mellor-Crummey, R. Fowler, and D. Whalley</p> <p>“Global Optimization Techniques for Automatic Parallelization of Hybrid Applications” D. R. Chakrabarti and Pr. Banerjee</p> <p>“Tuning High-Performance Scientific Codes: The Use of Performance Models to Control Resource Usage During Data Migration and I/O” J. Lee, M. Winslett, X. Ma and S. Yu</p> <p>“Computer Aided Hand Tuning (CAHT): ‘Applying Case-Based Reasoning to Performance Tuning’” A. Monsifrot and F. Bodin (20’)</p>		
9:30	<p><u>Session 1: Memory Models</u></p> <p>“Analytical Cache Models with Applications to Cache Partitioning.” G.E. Suh, S. Devadas and L. Rudolph</p> <p>“A Synthesis of Memory Mechanisms for Distributed Architectures” J. Zhu, J. Hoeflinger and D. Padua</p> <p>“The Trade-Off between Implicit and Explicit Data Distribution in Shared-Memory Programming Paradigms” D. S. Nikolopoulos, E. Ayguade, J. Labarta, T.S. Papatheodorou and C.D. Polychronopoulos</p>	<p><u>Session 4.2: Embedded Systems &amp; Special Applications</u></p> <p>“Cache Performance for Multimedia Applications” N. Slingerland and A.J. Smith</p> <p>On the Potential of Tolerant Region Reuse for Multimedia Applications” C. Alvarez, J. Corbal, E. Salami and M. Valero.</p> <p>“Evaluation of Processor Code Efficiency for Embedded Systems” M. H. Miki, M. Sakamoto, Y. Takeuchi, T. Yoshida, I. Shirakawa</p> <p>“Improving 3D Geometry Transformations on a Simultaneous Multithreaded SIMD Processor” C. Limousin, J. Sebot, A. Vartanian, N. Drach-Temam (20’)</p>		
10:50				
11:00	Coffee Break	Coffee Break		
11:30	<p><u>Session 2: Compilation I</u></p> <p>“Fractal Symbolic Analysis” N. Mateev, V. Menon and K. Pingali</p> <p>“Data Locality Enhancement by Memory Reduction,” Y. Song, R. Xu, C. Wang and Z. Li</p> <p>“Eliminating Redundancies in Sum-of-Product Array Computations,” S. J. Deitz, B.L. Chamberlain and L.Snyder</p>	<p><u>Panel 1: “Systems Software for Complex Computing Environments”</u></p> <p>Overview of the NSF Next Generation Software Program F. Darema , CISE Directorate, NSF</p> <p>An Integrated Framework for Performance Engineering and Resource-Aware Compiling System Constantine D. Polychronopoulos, William H. Sanders, Thomas Huang, Univ. of Illinois</p> <p>Compiling for Speculative Distributed Microarchitectures Rudolf Eigenmann - Purdue University; Babak Falsafi, Vijav Kumar</p> <p>Grid Application Development Software (GrADS) Ken Kennedy, Lennard Johnson, Andrew Chien, Keith Cooper, Francine Berman, Jack Dongarra, Dennis Gannon, Ian Foster, Carl Kesselman, Daniel A. Reed, Richard Wolski</p> <p>Supporting Complex Application Requirements in Metasystems Andrew Grimshaw, Marty Humphery, UVA</p> <p>Logistical QoS Through Application-driven Scheduling of Remote Storage James S. Plank, Jack Dongarra, Micah D. Beck, Richard Wolski - Univ. Of Tennessee; Francine D. Berman -UCSD</p> <p>Coordinated Allocation of Processor and I/O Resources in Parallel Systems Evgenia Smirni, College of William and Mary</p> <p>TMO Based Modeling &amp; Design of Reliable Next-Generation Complex Software Kane Kim, Phillip Chen Y Sheu; Michael Franz - Univ. of California, Irvine</p> <p>A Collaborative Problem Solving Environment for Modeling of Broadband Wireless Communication Systems Theodore S. Rapport, Clifford A. Shaffer, Layne T. Watson, Naren Ramakrishnan - VA Polytechnic Inst. &amp; University</p>		
13:00	Lunch Break	Conference Lunch		
14:30	<u>Invited:</u> Burton Smith (Cray): “What Happened to Supercomputers?”			
15:30	Coffee Break	& Pompeii Excursion		
16:00	<p><u>Session 3.1: Compilation II</u></p> <p>“Monotonic Evolution: an Alternative to Induction Variable Substitution for Dependence Testing” P. Wu, A. Cohen, D. Padua and J. Hoeflinger</p> <p>“Optimizing Strategies for Telescoping Languages: Procedure Strength Reduction and Procedure Vectorization” A. Chauhan and K. Kennedy</p> <p>“Loop Optimization for a Class of Memory-Constrained Computations” D. Cociorva J.W. Wilkins, C.C. Lam, G. Baumgartner, P. Sadayappan, J. Ramanujam</p>	<p><u>Session 3.2: Algorithms &amp; Sparse Computation</u></p> <p>“Fast Parallel In-memory 64-bit Sorting” D. Jimenez-Gonzalez, J.J. Navarro and J.J. Larriba-Pey</p> <p>“Optimizing Locality for ODE Solvers” T. Rauber and G. Ruenger (20’)</p> <p>“Array Language Support for Parallel Sparse Computation” B.L. Chamberlain and L. Snyder</p> <p>“A Parallel Algorithm for Sparse Symbolic LU Factorization without Pivoting on Out of Core Matrices” M. Cosnard and L. Grigori (20’)</p>		
17:30				
17:40	End of Day’s Technical Sessions			
19:30	Welcoming Reception			

Wednesday, June 20		Thursday, June 21	
9:00	<p><u>Session 5.1: Application Tools</u></p> <p>“Bringing Together Automatic Differentiation and OpenMP,” H.M. Buecker, B.L. Dieter, and M. H. Bischof</p>	<p><u>Session 5.2: Compilation &amp; Hw-Sw Interface</u></p> <p>“Register-Sensitive Selection, Duplication, and Sequencing of Instructions,” V. Sarkar, M. Serrano and B. Simons</p>	
9:30	<p>“Automatic Code Generation for a Turbulence Scheme,” P. v.d. Mark, G. Cats and L. Wolters (20’)</p> <p>“Towards Parallel Computation of Matrix Pseudospectra,” C. Bekas, E. Kokiopoulou and I. Koutis</p> <p>“A graphical tool for driving the parallel computation of the Pseudo-Spectra,” D. Mezher (20’)</p>	<p>“Load and Store Reuse using Register File Contents,” S. Onder and R. Gupta</p> <p>“Improving Gang Scheduling through Job Performance Analysis and Malleability,” J. Corbalan, X. Martorell and J. Labarta</p>	<p><u>Session 8: High Performance Java</u></p> <p>“Improving Java Performance Using Hardware Translation” R. Radhakrishnan, R. Bhargava and L. John</p> <p>“A Framework for Efficient Reuse of Binary Code in Java,” P.G. Joisha, S.P Midkoff, M.J. Serrano and M. Gupta</p>
10:30			
10:40	Coffee Break		
11:00	Coffee Break		
11:10	<p><u>Panel 2: “Dynamic Data Driven Applications”</u></p> <p>Model-Based Data Assimilation Greg McRae, MIT</p> <p>DDDAS Challenges in Managing Large-Scale Transportation and Supply Networks Abhi Deshmukh, Univ. of Massachusetts, Amherst</p> <p>Interactive Control of Large-Scale Simulations Robert Sharpley, University of South Carolina</p> <p>PDE-Constrained Optimization as an Enabling Technology for DDDAS Omar Ghattas, Carnegie-Mellon University</p> <p>Systems Software for Supporting DDDAS Environments Frederica Darema, NSF</p>	<p><u>Session 9.1: Load Balancing</u></p> <p>“Algorithmic modifications to the Jacobi-Davidson parallel eigensolver to dynamically balance external CPU and memory load” R.T. Mills, A. Stathopoulos and E. Smirni</p> <p>“Workload Decomposition for Particle Simulation Applications on Hierarchical Distributed-Shared Memory Parallel Systems with integration of HPF and OpenMP” S. Briguglio, B. Di Martino and G. Vlad</p>	<p><u>Session 9.2: Prefetching</u></p> <p>“ARIMA Time Series Modeling and Forecasting for Adaptive I/O Prefetching” N. Tran and D.A. Reed</p> <p>“Evaluating the Impact of Memory System Performance on Software Prefetching and Locality Optimizations” A.-H.A. Badawy, A. Aggarwal, D. Yeung, C.-W. Tseng</p> <p>“A novel renaming mechanism that boosts software prefetching” D. Ortega, M. Valero and E. Ayguadé</p>
12:00			
12:30			
12:40	Lunch Break		
14:10	<p><u>Session 6: Computer Architecture</u></p> <p>“Reducing the complexity of the issue logic,” R. Canal and A. Gonzalez</p> <p>“Slice-Processors: An Implementation of Operation-based Prediction,” A. Moshovos, D. Pnevmatikatos and A. Baniyadi</p> <p>“Building a High Performance Communication Layer over Virtual Interface Architecture on Linux Clusters,” J.-S. Kim, K. Kim, and S.-I. Jung</p> <p>“Integrating Superscalar Processor Components to Implement Register Caching,” M. Postiff, D. Greene, S. Raasch, and T. Mudge (20’)</p>		
16:00	<p><u>Invited: Gregory McRae (MIT): “New Directions for Data Assimilation”</u></p>		
17:00	Coffee Break		
17:30	<p><u>Parallel Session 7.1: High Performance Architecture &amp; Multithreading</u></p> <p>“a-Coral: A Multigrain, Multithreading Processor Architecture” M. Yankelevsky and C. D. Polychronopoulos (20’)</p> <p>“Multiplex: Unifying Conventional and Speculative Thread-Level Parallelism on a Chip Multiprocessor” C.-L. Ooi, S. Wook, K.I. Park, R. Eigenmann, B. Falsafi and T. N. Vijaykumar</p> <p>“Optimizing Threaded MPI Execution on SMP Clusters” H. Tang and T. Yang</p>	<p><u>Parallel Session 7.2: Computational Challenges</u></p> <p>“Demonstration of the Scalability of a Molecular Dynamics Application on a Petaflop Computer” G. Almasi, C. Cascaval, J.G. Castanos, M. Denneau, W. Donath, M. Eleftheriou, M. Giampapa, H. Ho, D. Lieber, J.E. Moreira, D. Newns, M. Snir and H.S. Warren Jr.</p> <p>“Computational Challenges in Large-scale Air Pollution Modelling” T. Ostromsky, W. Owczarz and Z. Zlatev</p> <p>“A network of cellular automata for landslide simulation,” C. R. Calidonna, C. Di Napoli, M. Giordano, M. Mango Furnari, S. Di Gregorio (20’)</p>	
18:50	End of Day’s Technical Sessions		
21:00	Conference Dinner		
			Conference Closing